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Docket No.: 60188-075

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Customer Number: 20277

Makoto FUJIWARA

Confirmation Number: 5700

Serial No.: 09/867,766

Group Art Unit: 2133

Filed: May 31, 2001

Examiner: not yet assigned

For:

JAN 0 7 2004

SEMICONDUCTOR INTEGRATED CIRCUIT AND METHOD OF TESTING

SEMICONDUCTOR INTEGRATED CIRCUIT

INFORMATION DISCLOSURE STATEMENT

RECEIVED

Mail Stop IDS Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

JAN 09 2004

MATERIAL STATES

Technology Center 2100

Dear Sir:

In accordance with the provisions of 37 C.F.R. 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the documents listed on the attached form PTO-1449. It is respectfully requested that the documents be expressly considered during the prosecution of this application, and that the documents be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is being filed within three months of the U.S. filing date OR before the mailing date of a first Office Action on the merits. No certification or fee is required.

09/867,766

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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INFORMATION DISCLOSURE CITATION IN AN APPLICATION							RIAL NO. 1/867,766		
JAN 0 7 2004					APPLICANT Makoto FUJIWARA				
(PTO-1449)					FILING DATE GROUP May 31, 2001 2133				
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1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.